PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Bednar et al.

Serial No.: 10/604,995

Filed: August 29, 2003

Title: Integrated Circuit Chip Having a Ringed Wiring Layer Interposed between a Contact Layer and a Wiring Grid

IBM Docket No.: BUR9200200107US1 (02016-00154)

Group Art Unit: Not yet assigned

Examiner: Not yet assigned

CERTIFICATE OF MAILING (37 C.F.R. 1.8a)

I hereby certify that this correspondence is, on the date shown below, being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, Alexandria, VA 22313-1450.

Morgan S. Heller II — 9/30/03 Date

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

September 30, 2003

Supplemental Information Disclosure Statement Transmittal

In connection with the above-identified application, please find attached a supplement to the Information Disclosure Statement filed on August 29, 2003, along with a copy of the reference cited therein.

This Information Disclosure Statement is being submitted within three months of the filing date of the present application. Therefore no fee is due in connection with this submission.

If any other fee is due with respect to the present application, please charge, or credit any overcharge, to Deposit Account No. 09-0456.

P242-12/00

Law Offices of
Downs Rachlin Martin PLLC
199 Main Street
P.O. Box 190
Burlington, VT 05402-0190
(802) 863-2375

Respectfully submitted,

DOWNS RACHLIN MARTIN PLLC

By: 

Morgan S. Heller II
Attorney of Record
Registration No.: 44,756
Tel: (802) 863-2375

BTV/245689.1

P242-12/00

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P.O. Box 190
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INFORMATION DISCLOSURE STATEMENT FILED PURSUANT TO THE DUTY OF DISCLOSURE UNDER 37 C.F.R. §§1.56, 1.97 AND §1.98

Pursuant to the duty of disclosure under 37 C.F.R. §§1.56, 1.97 and §1.98, applicants request consideration of this Information Disclosure Statement.

Information Cited

Applicants hereby make of record in the above-identified application the information listed on the attached form PTO-1449 (modified). The order of presentation of the references should not be construed as an indication of the importance of the references.

REMARKS

A copy of each of the above-identified items of information is enclosed unless otherwise indicated on the attached form PTO-1449 (modified). It is respectfully requested that:

1. the examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. the enclosed form PTO-1449 be signed by the examiner to evidence that the cited information has been fully considered by the Patent and Trademark Office during the examination of this application; and

3. the citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, applicants make no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.

By submitting this Information Disclosure Statement, applicants make no representation that the information cited in this Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. §1.56(b).

By submitting this Information Disclosure Statement, applicants make no representation that the information cited in this Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. §102.

Notwithstanding any statements by applicant, the examiner is urged to form his/her own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

Respectfully submitted,

DOWNS RACHLIN MARTIN PLLC

By: _____

Morgan S. Heller II
Reg. No. 44,756
(802) 863-2375

FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S *SUPPLEMENTAL* INFORMATION DISCLOSURE STATEMENT

Page 1 of 1

(Use several sheets if necessary.)

ATTY DOCKET NO.	SERIAL NO.
BUR9200200107US1	10/604,995
APPLICANT: Bednar et al.	
FILING DATE: 8/29/2003	GROUP: Not yet assigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
	AO						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AO							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AP		INCREASED CHIP WIREABILITY THROUGH MORE EFFICIENT POWER DISTRIBUTION, IBM Technical Disclosure Bulletin, Vol. 38, No. 09, pgs. 243-245, September 1995.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.